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5 providing each transaction with a transaction identification value to determine  
an order of execution of each transaction;

gathering transactions having an identical master identification value and accessing the shared system resource in sequence according to the transaction identification value.

3. The method of claim 2, wherein the step of providing each transaction with the transaction identification value includes the sub-steps of:

adding 0 to the transaction identification value when the previous transaction of the read transaction is the write transaction;

adding 0 to the transaction identification value when the previous transaction of the write transaction is the write transaction.

4. The method of claim 3, wherein the step of accessing the shared system resource according to the transaction identification value includes the sub-steps of:

picking up the transaction having the smallest transaction identification value and executing the transaction to access the shared system resource; and

5       executing the write transactions to access the shared system resource before the read transactions if two or more transactions have the same smallest transaction identification value.

10       5. The method of claim 1, wherein the sequencing method also incorporates a flush and a fence signal provided by an accelerated graphic port (AGP) bus to ensure proper transaction execution sequence.

6. A bridging system for accessing a shared system resource, comprising:

at least one master controller, wherein the at least one master controller is capable of submitting a plurality of write transactions and a plurality of read transactions;

15       a first bus coupled to the at least one master controller;

a bridging device coupled to the first bus for transporting the read transactions and the write transactions;

a second bus coupled to the bridging device; and

20       a chipset coupled to the second bus and the shared system resource for selecting one of the read transactions or the write transactions initiated from one of the at least one master controller so that the shared system resource is accessed.

7. The bridging system of claim 6, wherein the first bus is a PCI bus.

8. The bridging system of claim 6, wherein the second bus is an accelerated graphic port (AGP) bus.

Sub

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a read queue for holding the master identification values and the transaction identification values of all read transactions;

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identification value; and

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